







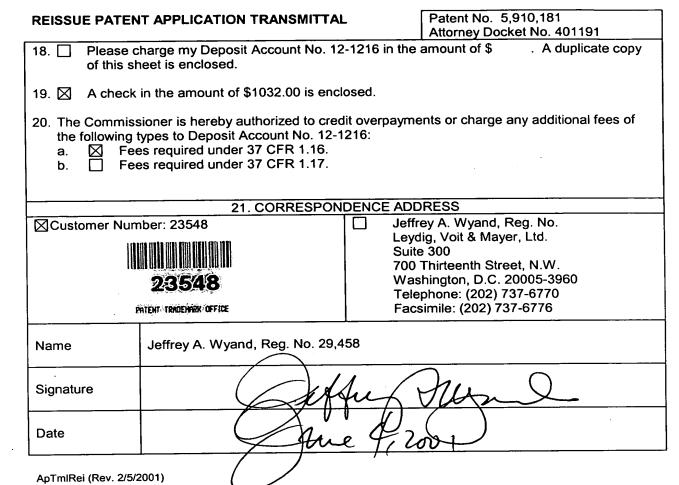
| REISSUE PATENT APPL | ICATION TRAN | SMITTAL | a _d | | |
|---|---|--|----------------|--|--|
| ADDRESS TO: | RESS TO: Attorney Docket No. | | .97. | | |
| | First Named Inventor | Makoto Hatakenaka | 3.E | | |
| Commissioner for Patents Box Reissue | Original Patent No. | 5,910,181 | 9/8 | | |
| Washington, D.C. 20231 | Original Patent Issue Date (Month/Day/Year) | 6/8/99 | 3C9 | | |
| | Express Mail Label No. | | | | |
| APPLICATION FOR REISSUE OF: Utility Pa (Check applicable box) | atent | nt | | | |
| APPLICATION ELEMENTS | ACCOMPANYING APPLICATION PARTS | | | | |
| Transmittal Form with Fee Applicant claims small entity status. See Transmittal Form with Fee Applicant claims small entity status. See | 7. Statement of status/support for all changes to the claims. See 37 CFR 1.173(c) | | | | |
| 3. Specification and Claims in double column copy of patent format (amended, if appropriate) | 8. Original U.S. Pate | ent for surrender Original Patent Grant | | | |
| Statement of Loss (PTO/SB/55) | | | | | |

Instructions for Calculating Claim Fees:

If Total Claims In Patent is greater than 20, use Number Filed In Reissue Application minus Total Claims In Patent; if Claims In Patent is less than 20, use Number Filed In Reissue Application minus 20.

| CLAIMS AS FILED - PART 1 | | | | | | | | |
|---|---------------------|-------------------------------------|-----------------|---------------|-----------|--|--|--|
| BASIC FEE | | | | | | | | |
| | CLAIMS IN PATENT | NUMBER FILED IN REISSUE APPLICATION | NUMBER EXTRA | RATE | | | | |
| TOTAL CLAIMS | 9 | 18 | 9 | x\$18.00 | \$ 162.00 | | | |
| INDEPENDENT CLAIMS | 2 | 4 | 2 | x\$80.00 | \$ 160.00 | | | |
| | | Tot | al of above c | alculations = | \$1032.00 | | | |
| Reduction by 50% for filing by small entity = | | | | | (\$) | | | |
| TOTAL = | | | | | \$1032.00 | | | |

| | CLAIMS A | AS AMENDED - PAI | RT 2 | | | |
|---|------------------|------------------|-------------|---------------|-----|---------------|
| | | HIGHEST NUMBER | EXTRA | | | |
| | CLAIMS REMAINING | PREVIOUSLY PAID | CLAIMS | | | |
| <u>.</u> | AFTER AMENDMENT | For | PRESENT | RATE | | |
| TOTAL CLAIMS | | | 0 | x\$18.00 | \$ | |
| INDEPENDENT CLAIMS | | | | x\$80.00 | \$ | |
| | | Tota | of above ca | alculations = | \$ | |
| Reduction by 50% for filing by small entity = | | | | | (\$ |) |
| | | *\ | | TOTAL = | \$ | |
| | | | | | 0 | |



Patent Attorney Docket No. 401191

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U. S. Patent 5,910,181 of:

HATAKENAKA et al.

Application No.: Unassigned

Art Unit:

Unassigned

Filed:

June 4, 2001

Examiner:

Unassigned

For:

SEMICONDUCTOR INTEGRATED CIRCUIT COMPRISING SYNCHRON-OUS DRAM CORE AND LOGIC CIRCUIT INTEGRATED INTO A SINGLE CHIP AND METHOD OF TESTING THE SYNCHRON-

OUS DRAM CORE

ASSENT OF ASSIGNEE AND OFFER TO SURRENDER

Commissioner for Patents Washington, D. C. 20231

Dear Sir:

In accordance with 37 C.F.R. §1.172, Mitsubishi Denki Kabushiki Kaisha., Assignee and owner of the entire interest in United Patent 5,910,181 to Hatakenaka et al., for "Semiconductor Integrated Circuit Device Comprising Synchronous DRAM Core And Logic Circuit Integrated Into A Single Chip And Method Of Testing The Synchronous DRAM Core", assents to the filing of the accompanying reissue patent application and the reissue declaration signed by the inventor.

In accordance with the provisions of 37 C.F.R. §1.178, the Applicant for reissue of United State Patent 5,910,181 for "Semiconductor Integrated Circuit Device Comprising Synchronous DRAM Core And Logic Circuit Integrated Into A Single Chip And Method Of Testing The Synchronous DRAM Core", granted on June 8, 1999, naming Makoto

In re Application of Hatakenaka et al. Application No. Unassigned

Hatakenaka, Akira Yamazaki, Shigeki Tomishima, and Tadato Yamagata as inventors, and assigned to Mitsubishi Denki Kabushiki Kaisha, offers to surrender the original Letters Patent upon allowance of the reissue patent application.

There are no concurrent proceedings in the United States Patent and Trademark Office concerning United States Patent 5,910,181, such as interferences, other reissue applications, or re-examinations, and no pending litigations in any forum.

I certify that the invention disclosed in United States Patent 5,910,181 is assigned by the inventors, Makoto Hatakenaka, Akira Yamazaki, Shigeki Tomishima, and Tadato Yamagata to Mitsubishi Denki Kabushiki Kaisha in an assignment dated October 20 and 27, 1997 and recorded in the assignment records of the United States Patent and Trademark Office at Reel 8879, Frame 0949 on November 4, 1997.

I state that I am authorized to act on behalf of Mitsubishi Denki Kabushiki Kaisha in offering to surrender the original Letters Patent, to request reissue of the original Letters Patent, and to verify the ownership of the patent.

MITSUBISHI DENKI KABUSHIKI KAISHA

y your

General Manager

Patent Administration Department

Date: May 24, 200/

Patent
Attorney Docket No. 401191
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U. S. Patent 5,910,181 of:

HATAKENAKA et al.

Application No.: Unassigned

Art Unit:

Unassigned

Filed:

June 4, 2001

Examiner:

Unassigned

For:

SEMICONDUCTOR INTEGRATED CIRCUIT COMPRISING SYNCHRON-OUS DRAM CORE AND LOGIC CIRCUIT INTEGRATED INTO A SINGLE CHIP AND METHOD OF TESTING THE SYNCHRON-

OUS DRAM CORE

REQUEST FOR TRANSFER OF DRAWINGS FOR REISSUE APPLICATION

Commissioner for Patents Washington, D. C. 20231

Dear Sir:

In accordance with 37 C.F.R. §1.172, the Reissue Applicant requests that the drawings for United States Patent 5,910,181 corresponding to Application Serial Number 08/964,236, filed November 4, 1997, be transferred to the reissue patent application. Fifteen sheets of drawings are attached for examination purposes.

Respectfully submitted,

ŁEXDIG, VOIT & MAYER, LTD.

Registration No. 29,458

Suite 300

700 Thirteenth Street, N. W. Washington, D. C. 20005

Telephone: (202) 737-6770 Facsimile, (202) 737-6776

Date: / Me

wi